

In the Claims

Please amend the claims as follows:

1           1. (Currently Amended) A method of data transfer between a  
2 source port and a destination port of a transfer controller with  
3 plural ports, said method comprising the steps of:

4           in response to a data transfer request, querying said  
5 destination port to determine if said destination port is capable  
6 of receiving data of a predetermined size;

7           if said destination port is not capable of receiving data of  
8 said predetermined size, waiting by not reading data of said  
9 predetermined size from said source port corresponding to said data  
10 transfer request, not storing data read from said source port in  
11 intermediate buffers and not transferring data to said destination  
12 port thereby not blocking reading data from said source port until  
13 said destination port is capable of receiving data; ~~and~~

14           if said destination port is capable of receiving data of said  
15 predetermined size, reading data of said predetermined size from  
16 said source port and transferring said read data to said  
17 destination port; and

18           while waiting until said destination port is capable of  
19 receiving data

20                 determining if a second data transfer request is pending  
21 between said source port and a second destination port, and

22                 if a second data transfer request is pending

23                     querying said second destination port to determine  
24 if said second destination port is capable of receiving  
25 data of said predetermined size,

26                     if said second destination port is not capable of  
27 receiving data of said predetermined size, waiting by not  
28 reading data of said predetermined size from said source  
29 port corresponding to said second data transfer request,

30       not storing data read from said source port in  
31       intermediate buffers and not transferring data to said  
32       second destination port thereby not blocking reading data  
33       from said source port until said second destination port  
34       is capable of receiving data, and  
35               if said second destination port is capable of  
36       receiving data of said predetermined size, reading data  
37       of said predetermined size from said source port and  
38       transferring said read data to said second destination  
39       port.

1       2. (Currently Amended) The method of claim 1, wherein each  
2 port includes at least one write reservation station, said method  
3 wherein:

4       said step of querying said destination port includes:  
5               determining whether any write reservation station capable  
6       of storing data of said predetermined size of said destination  
7       port has not been allocated for receipt of data,  
8               if at least one write reservation capable of storing data  
9       of said predetermined size is not allocated for receipt of  
10       data, determining said destination port can receive data and  
11       allocating a write reservation station capable of storing data  
12       of said predetermined size for receipt of data; and  
13       said step of transferring said read data to said destination  
14 port includes transferring said read data to said allocated write  
15 reservation station of said destination port.

1       3. (Original) The method of claim 2, further comprising:  
2       transferring data from a write reservation station storing  
3 data to be transferred to an application unit coupled to said  
4 destination port at a data transfer rate of said application unit;  
5 and

6        disallocating said write reservation station upon transfer of  
7        data to said application unit.

1        4. (Original) The method of claim 2, wherein:

2        said step of allocating a write reservation station includes  
3        storing a data identifier corresponding to said write reservation  
4        station; and

5        said step of transferring said read data to said destination  
6        port includes storing said read data in a write reservation station  
7        having a data identifier corresponding to said read data.

Claims 5 and 6. (Canceled)

1        7. (Currently Amended) A data transfer controller comprising:

2        a request queue controller receiving, prioritizing and  
3        dispatching data transfer requests, each data transfer request  
4        specifying a data source, a data destination and a data quantity to  
5        be transferred;

6        a data transfer hub connected to request queue controller  
7        effecting dispatched data transfer requests;

8        a plurality of ports, each of said plurality of ports having  
9        an interior interface connected to said data transfer hub and an  
10       exterior interface configured for an external memory/device  
11       expected to be connected to said port, said interior interface and  
12       said exterior interface operatively connected for data transfer  
13       therebetween; and

14       said data transfer hub controlling data transfer from a source  
15       port corresponding to said data source to a destination port  
16       corresponding to said data destination in a quantity corresponding  
17       to said data quantity to be transferred of a currently executing  
18       data transfer request, said data transfer hub further controlling  
19       said source port and said destination port to

20 in response to a data transfer request, query said  
21 destination port to determine if said destination port is  
22 capable of receiving data of a predetermined size,

23 if said destination port is not capable of receiving data  
24 of said predetermined size, waiting by not reading data of  
25 said predetermined size from said source port corresponding to  
26 said data transfer request and not transferring data to said  
27 destination port thereby not blocking reading data from said  
28 source port until said destination port is capable of  
29 receiving data, and

30 if said destination port is capable of receiving data of  
31 said predetermined size, reading data of said predetermined  
32 size from said source port and transferring said read data to  
33 said destination port, and

34 said data transfer hub further capable while waiting until  
35 said destination port is capable of receiving data of

36 determining if a second data transfer request between  
37 said source port and a second destination port is pending,

38 if a second data transfer request is pending

39 querying said second destination port to determine  
40 if said second destination port is capable of receiving  
41 data of said predetermined size,

42 if said second destination port is not capable of  
43 receiving data of said predetermined size, waiting by not  
44 reading data of said predetermined size from said source  
45 port corresponding to said second data transfer request  
46 thereby not blocking reading data from said source port  
47 until said second destination port is capable of  
48 receiving data, and

49 if said second destination port is capable of  
50 receiving data of said predetermined size, reading data  
51 of said predetermined size from said source port and

52           transferring said read data to said second destination  
53           port.

1           8. (Currently Amended) The data transfer controller of claim  
2   7, wherein:  
3           each port includes at least one write reservation station for  
4   storing data prior to transfer to said corresponding external  
5   memory/device;  
6           said data transfer hub further controlling said destination  
7   port to  
8           determine whether any write reservation station capable  
9           of storing data of said predetermined size of said destination  
10   port has not been allocated for receipt of data,  
11           if at least one write reservation capable of storing data  
12           of said predetermined size is not allocated for receipt of  
13   data, determining said destination port can receive data and  
14   allocating a write reservation station capable of storing data  
15           of said predetermined size for receipt of data, and  
16           transfer said read data to said allocated write  
17   reservation station of said destination port.

1           9. (Original) The data transfer controller of claim 8,  
2   wherein:  
3           said data transfer hub further controlling said destination  
4   port to  
5           transfer data from a write reservation station to said  
6   corresponding external memory/device at a data transfer rate  
7   of said external memory/device, and  
8           disallocating said write reservation station upon  
9   transfer of data from said write reservation station to said  
10   external memory/device.

1        10.    (Previously Amended) The data transfer controller of  
2 claim 8, wherein:

3        each of said plurality of ports further includes an identifier  
4 register corresponding to each write reservation station; and  
5        said data transfer hub further controlling said destination  
6 port to

7            allocate a write reservation station by writing  
8 identifier data in said corresponding identifier register, and  
9            store said read data in a write reservation station  
10 having a corresponding identifier stored in said identifier  
11 register corresponding to said write reservation station.

Claims 11 and 12    (Canceled).

1        13.    (Currently Amended) A data processing system comprising:  
2 a plurality of data processors, each data processor capable of  
3 generating a data transfer request;

4        a request queue controller connected to said plurality of data  
5 processors, said request queue controller receiving, prioritizing  
6 and dispatching data transfer requests, each data transfer request  
7 specifying a data source, a data destination and a data quantity to  
8 be transferred;

9        a data transfer hub connected to request queue controller  
10 effecting dispatched data transfer requests;

11        a plurality of ports, each of said plurality of ports having  
12 an interior interface connected to said data transfer hub  
13 identically configured for each port and an exterior interface  
14 configured for an external memory/device expected to be connected  
15 to said port, said interior interface and said exterior interface  
16 operatively connected for data transfer therebetween; and

17        said data transfer hub controlling data transfer from a source  
18 port corresponding to said data source to a destination port

19 corresponding to said data destination in a quantity corresponding  
20 to said data quantity to be transferred of a currently executing  
21 data transfer request, said data transfer hub further controlling  
22 said source port and said destination port to

23       in response to a data transfer request, query said  
24 destination port to determine if said destination port is  
25 capable of receiving data of a predetermined size,

26       if said destination port is not capable of receiving data  
27 of said predetermined size, waiting by not reading data of  
28 said predetermined size from said source port corresponding to  
29 said data transfer request and not transferring data to said  
30 destination port thereby not blocking reading data from said  
31 source port until said destination port is capable of  
32 receiving data, and

33       if said destination port is capable of receiving data of  
34 said predetermined size, reading data of said predetermined  
35 size from said source port and transferring said read data to  
36 said destination port, and

37 said data transfer hub further capable while waiting until  
38 said destination port is capable of receiving data of

39 determining if a second data transfer request between  
40 said source port and a second destination port is pending,

41 if a second data transfer request is pending

42 querying said second destination port to determine  
43 if said second destination port is capable of receiving  
44 data of said predetermined size,

45 if said second destination port is not capable of  
46 receiving data of said predetermined size, waiting by not  
47 reading data of said predetermined size from said source  
48 port corresponding to said second data transfer request  
49 thereby not blocking reading data from said source port

50           until said second destination port is capable of  
51           receiving data, and  
52           if said second destination port is capable of receiving  
53           data of said predetermined size, reading data of said  
54           predetermined size from said source port and transferring said  
55           read data to said second destination port.

1           14. (Currently Amended) The data processing system of claim  
2   13, wherein:

3           each port includes at least one write reservation station for  
4   storing data prior to transfer to said corresponding external  
5   memory/device;

6           said data transfer hub further controlling said destination  
7   port to

8           determine whether any write reservation station capable  
9           of storing data of said predetermined size of said destination  
10   port has not been allocated for receipt of data,

11           if at least one write reservation capable of storing data  
12           of said predetermined size is not allocated for receipt of  
13   data, determining said destination port can receive data and  
14   allocating a write reservation station capable of storing data  
15           of said predetermined size for receipt of data, and

16           transfer said read data to said allocated write  
17   reservation station of said destination port.

1           15. (Original) The data processing system of claim 14,  
2   wherein:

3           said data transfer hub further controlling said destination  
4   port to

5           transfer data from a write reservation station to said  
6   corresponding external memory/device at a data transfer rate  
7   of said external memory/device, and



8            disallocate said write reservation station upon transfer  
9            of data from said write reservation station to said external  
10           memory/device.

1           16.   (Original) The data processing system of claim 14,  
2   wherein:  
3           each of said plurality of hubs further includes an identifier  
4   register corresponding to each write reservation station; and  
5           said data transfer hub further controlling said destination  
6   port to  
7           allocate a write reservation station by writing  
8   identifier data in said corresponding identifier register, and  
9           store said read data in a write reservation station  
10   having a corresponding identifier stored in said identifier  
11   register corresponding to said write reservation station.

Claims 17 and 18   (Canceled)

1           19.   (Previously Amended) The data processing system of claim  
2   13, further comprising:  
3           said plurality of ports includes an internal port master;  
4           a data transfer bus connected to said internal port master and  
5   each of said data processors, said data transfer bus transferring  
6   data between said plurality of data processors and said data  
7   transfer hub via said internal port master;  
8           a system memory connected to a predetermined one of said  
9   plurality of ports; and  
10          wherein each of said data processors includes an instruction  
11   cache connected to said data transfer bus for temporarily storing  
12   program instructions controlling said data processor, said data  
13   processor generating a data transfer request to said request queue  
14   controller for instruction cache fill from said system memory to

15 said instruction cache upon a read access miss to said instruction  
16 cache.

1 20. (Previously Amended) The data processing system of claim  
2 13, further comprising:

3 said plurality of ports includes an internal port master;  
4 a data transfer bus connected to said internal port master and  
5 each of said data processors, said data transfer bus transferring  
6 data between said plurality of data processors and said data  
7 transfer hub via said internal port master;

8 a system memory connected to a predetermined one of said  
9 plurality of ports; and

10 wherein each of said data processors includes a data cache  
11 connected to said data transfer bus for temporarily storing data  
12 employed by said data processor, said data processor generating a  
13 data transfer request to said request queue controller for data  
14 cache fill from said system memory to said data cache upon a read  
15 access miss to said data cache.

1 21. (Previously Amended) The data processing system of claim  
2 13, further comprising:

3 said plurality of ports includes an internal port master;  
4 a data transfer bus connected to said internal port master and  
5 each of said data processors, said data transfer bus transferring  
6 data between said plurality of data processors and said data  
7 transfer hub via said internal port master;

8 a system memory connected to a predetermined one of said  
9 plurality of ports; and

10 wherein each of said data processors includes a data cache  
11 connected to said data transfer bus for temporarily storing data  
12 employed by said data processor, said data processor generating a  
13 data transfer request to said request queue controller for data

14 writeback from said data cache to said system memory upon a write  
15 miss to said data cache.

1        22. (Previously Amended) The data processing system of claim  
2 13, further comprising:  
3        said plurality of ports includes an internal port master;  
4        a data transfer bus connected to said internal port master and  
5 each of said data processors, said data transfer bus transferring  
6 data between said plurality of data processors and said data  
7 transfer hub via said internal port master;  
8        a system memory connected to a predetermined one of said  
9 plurality of ports; and  
10       wherein each of said data processors includes a data cache  
11 connected to said data transfer bus for temporarily storing data  
12 employed by said data processor, said data processor generating a  
13 data transfer request to said request queue controller for write  
14 data allocation from said system memory to said data cache upon a  
15 write miss to said data cache.

1        23. (Previously Amended) The data processing system of claim  
2 13, further comprising:  
3        said plurality of ports includes an internal port master;  
4        a data transfer bus connected to said internal port master and  
5 each of said data processors, said data transfer bus transferring  
6 data between said plurality of data processors and said data  
7 transfer hub via said internal port master;  
8        a system memory connected to a predetermined one of said  
9 plurality of ports; and  
10       wherein each of said data processors includes a data cache  
11 connected to said data transfer bus for temporarily storing data  
12 employed by said data processor, said data processor generating a  
13 data transfer request to said request queue controller for data

14 writeback from said data cache to said system memory upon eviction  
15 of dirty data from said data cache.

1 24. (Original) The data processing system of claim 13,  
2 wherein:

3 said plurality of data processors, said request queue  
4 controller, said data transfer hub and said plurality of ports are  
5 disposed on a single integrated circuit.

1 25. (Currently Amended) The data processing system of claim  
2 13, further comprising:

3 a data memory having a data transfer bandwidth on the same  
4 order as a data transfer bandwidth of said data transfer hub;

5 an internal memory port connected to said data transfer hub  
6 and said data memory; and

7 said data transfer hub further controlling said source port  
8 and said destination port to not query said internal memory port to  
9 determine if said destination port is capable of receiving data of  
10 a predetermined size, read data of said predetermined size from  
11 said source port and transfer said read data to said destination  
12 port via said data transfer hub if said internal memory port is a  
13 destination port of a data transfer request.